Jan Marjanovič

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Summary

An FPGA developer with 9+ years of experience in electronic instrumentation for experimental physics with a track record of delivering high-quality products used in mission-critical applications at the world's largest and most advanced facilities. Enthusiastic about tackling the complexity of parallelism in FPGA with new programming languages and paradigms, e.g. Chisel and High-Level Synthesis.

Work Experience

FPGA Consultant, Hamburg, Germany

Apr 2022 - Present

Clients:

- Atom Computing, Inc.

Deutsches Elektronen-Synchrotron DESY, Hamburg, Germany

Senior FPGA Developer **Jan 2021 - Mar 2022**

- Coordinated the bring-up of a **Zynq UltraScale+ MPSoC**-based FMC/FMC+ carrier, led the development of a Board Support Package; this board became a very popular platform in the broader community
- Implemented a data acquisition design on Zynq UltraScale+ MPSoC with a high-speed **LVDS** interface, **AXI4 DMA**, **PCI Express**, and **DDR4** memory used for special diagnostics at our particle accelerators
- Participated as an FPGA expert in the development of a phasemeter in a collaboration with a university
- Held presentations and tutorials at intl. workshops and conferences (full list: https://www.desy.de/~jmarjan/)

FPGA Developer **Aug 2017 - Dec 2020**

- Co-developed a UDP/IPv4 IP for **1Gb/10Gb Ethernet** and an FPGA-based (10)GigE Vision implementation
- Developed an image processing IP with **Vivado HLS** used in high-end scientific and industrial applications
- Conceived and conducted **MicroTCA** training course (2+2 days) in collaboration with a colleague; taught hundreds of technicians, engineers and scientists on how to use MicroTCA and related technologies
- Developed a Board Support Package for a **Xilinx Kintex-7**-based communication card
- Prepared the design for the evaluation of **Xilinx RFSoC**, participated in the measurement campaign
- Participated in several successful troubleshooting sessions for internal and external customers

CAEN ELS s.r.l., Trieste, Italy and Sežana, Slovenia

R&D Engineer **May 2014 - Jul 2017**

- Developed an FPGA-based feedback controller in **Vivado HLS** on **Xilinx Zynq-7000** for a family of advanced power supplies, used both in industry and as a mission-critical component in some large synchrotrons
- Developed an **AXI4** interconnect and a DMA for **PCI Express** on **Xilinx Virtex-5** for a picoammeter in MicroTCA form factor, wrote the initial version of the Linux driver
- Integrated a UDP/IPv4 engine in a multi-FPGA system with **Altera Cyclone V**, developed an advanced feedback controller used to significantly improve photon flux at the sample at beamlines
- Occasionally accompanied salespeople, held presentations at international workshops

Student Worker **Feb 2013 - May 2014**

- Developed a data acquisition system with **Altera Cyclone IV** and **Nios II** for a picoammeter; this later became a very successful product, used at numerous institutes and companies all around the world

Education

University of Ljubljana (Slovenia)
Diploma (equivalent to **Master's Degree**) in **Electrical Engineering**

Oct 2008 - Jan 2013, graduated in May 2014

Thesis Title: System on Chip for Load Identification on a Switching Power Supply

Final grade average: 9.667 (out of 10), *Thesis grade*: 10 (out of 10)

Received awards and scholarships: The Award of the Dean for exemplary completion of study requirements in Year 1 of the university study programme, The Award for excellent final grade upon the completion of studies, Zois scholarship for students with extraordinary achievements

Publication: J. Marjanovic, A. Trost: *System on Chip for Load Identification on a Switching Power Supply*, MIDEM Conference, 2014, Ljubljana

Skills

Languages and frameworks

- SystemVerilog and VHDL
- UVVM, Xilinx VIPs
- C, C++, Python, Tcl
- Chisel

Technologies

- Xilinx Zynq UltraScale+ MPSoC, Xilinx 7-series, Intel Stratix V
- PCI Express, Ethernet
- AMBA AXI, Intel/Altera Avalon
- MicroTCA, IPMI, Linux

Tools

- Xilinx Vivado, Vivado HLS
- Intel Quartus, Nios II EDS
- ModelSim and Questa
- Git, Docker, Jenkins
- Yocto

Personal Projects

- Chisel Bus Functional Model tester and a collection of Chisel projects
- Reverse engineering of Microsoft Pikes Peak/Storey Peak FPGA card (based on Intel Stratix V)
- Jan's RISC-V Playground: a simple SW emulator, an RV32I core, a prototype of a scalar pipeline

Languages

- **English** - Full professional proficiency
- **German** - Elementary proficiency
- **Italian** - Full professional proficiency
- **Slovenian** - Native proficiency